Session 4 Overview

Gigabit Transceivers

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This session covers recent advances in CMOS gigabit transceivers and equalization techniques for a variety of electrical interconnects: short-distance chip-to-chip, backplane, shielded and unshielded twisted pair (UTP) cables. Each application brings a unique set of bandwidth limitation challenges and equalization requirements. The equalization varies from a simple TX pre-emphasis to an adaptive multi-tap FIR solution in combination with multi-tap DFE receivers. Multi-gigabit signaling over UTP cables requires a PAM-4 modulation while more traditional channels are NRZ-based. Once the data rate starts approaching 10 to 20Gb/s the equalization becomes important in traditional chip-to-chip interfaces.

In Paper 4.1, a 10Gb/s 5-tap-DFE/4-tap-FFE transceiver, addresses up to 20 inch back-plane applications while consuming only 300mW from a 1.2V supply. The main design enhancements are related to the reduction of the DFE response time and the improvement of the timing recovery precision.

The most common equalizers attempt to drive the ISI to zero at the center of the data eye. One question that often arises in transceiver design is whether providing additional equalization at the crossing points is beneficial. This problem is studied for both transmit and receive equalizers in Paper 4.2.

One of the major challenges transceivers must overcome is operation in the presence of crosstalk. One way to mitigate this problem is edge-rate control. An effective 1.5Gb/s to 6Gb/s multi-rate solution is provided in Paper 4.3. Each channel employs analog-type CDR with capacitance multiplication in the charge-pump filter.

The most challenging design problem is achieving multi-gigabit data transmission through 4 pairs of UTP cable. In Paper 4.4, a 12.5Gb/s analog-based single-chip transceiver for 25m of CAT-6 cable with only a 3.8W power dissipation is discussed.

In Papers 4.5 and 4.6, chip-to-chip interfaces with equalization techniques traditionally used for longer interconnects are discussed. To reduce power dissipation in a 20Gb/s transceiver, Paper 4.6 proposes to forward the clock in a separate channel while data alignment is achieved with a local DLL.

In Paper 4.7, a spectrum-balancing technique for equalizer adaptation at 20Gb/s is explored. It does not require a slicer in the equalization path and reduces power down to 60mW.

Finally, an integrated transformer-based solution to overcome the power-supply limitation of traditional TX pre-emphasis, where low frequencies are de-emphasized, is suggested. Integrated transformers typically are not suitable for a direct data path due to their narrow-band characteristics. However, they are well positioned for implementing TX pre-emphasis within one 8Gb/s data bit interval.

4.1 A 10Gb/s 5-Tap-DFE/4-Tap-FFE Transceiver in 90nm CMOS **1:30 PM**

M. Meghelli, IBM, Yorktown Heights, NY

A 90nm CMOS 10Gb/s SerDes for chip-to-chip communications over backplanes is presented. To mitigate channel impairments, the RX uses a 5-tap DFE and the TX a 4-tap FIR filter. The IC equalization abilities are evaluated using different type of channels. The power consumption of one (TX, RX) pair and one PLL is 300mW for $1.2V_{pp}$ differential TX output swing.

4.2 A Serial-Link Transceiver with Transition Equalization **2:00 PM**

K. Wong, University of California, Los Angeles, CA

Two transition-equalization techniques are proposed. A pulse-overlapping half-symbol tap FIR transmitter is able to equalize a 120-inch 40dB attenuation FR4 with BER of $<10^{-13}$ at 3.7Gb/s. A DFE with transition ISI cancellation performs better than traditional DFE and achieves a BER of $<10^{-12}$ at 3.6Gb/s with 80-inch FR4

4.3 A Quad 6Gb/s Multi-rate CMOS Transceiver with TX Rise/Fall-Time Control **2:30 PM**

Y. Moon, Silicon Image, Sunnyvale, CA

A multi-rate transceiver incorporating TX slew control with >2x range, PLL with <0.5x loop-filter area using capacitance multiplication, and ΔΣ-SSCG having 11.7dB peak reduction is designed in 0.13µm CMOS. Occupying $2.33mm^2$ with TX operable up to 8.5Gb/s, the quad transceiver consumes 386mW from 1.2V supply and has a BER$<10^{-14}$ at 6Gb/s over an 8m cable with 22dB loss.

4.4 A 12.5Gb/s Single-Chip Transceiver for UTP Cable in 0.13µm CMOS **3:15 PM**

M. Callicotte, Keyeye Communications, Sacramento, CA

The demand for multi-Gb transceivers over copper medium is rapidly increasing. While this function is currently accomplished by fiber-optic transceivers, their high cost and difficult installation makes other possible alternatives attractive. A 0.13µm CMOS solution consuming 3.8W at a maximum data-rate of 12.5Gb/s is presented.

4.5 A 100mW 9.6Gb/s Transceiver in 90nm CMOS for Next-Generation Memory Interfaces **3:45 PM**

E. Prete, Infineon, Munich, Germany

An architecture for next-generation memory interface is demonstrated using 90nm bulk silicon to provide a 2-tap emphasized TX with <19ps jitter at 9.6Gb/s. The circuit uses a programmable PLL to track jitter up to 200MHz. The transceiver consumes 100mW from a 1V supply.

4.6 A 20Gb/s Forwarded Clock Transceiver in 90nm CMOS **4:15 PM**

B. Casper, Intel, Hillsboro, OR

A forwarded clock I/O link in 90nm CMOS is capable of passing data at 20Gb/s over 7-inches of FR4 with 2 sockets and packages at a power dissipation of less than 12mW/Gb/s. Passive distribution and AC coupling of the forwarded clock are used to achieve $820fs_{rms}$ of sample-time uncertainty. Nyquist rate channel losses in excess of -15dB are compensated using a combination of 4-tap transmit equalization and receiver continuous-time equalization.

4.7 A 20Gb/s Adaptive Equalizer in 0.13µm CMOS Technology **4:45 PM**

J. Lee, National Taiwan University, Taipei, Taiwan

An adaptive equalizer incorporates a spectrum-balancing technique to achieve high speed and low power obviating the need for slicers. Fabricated in 0.13µm CMOS, this circuit achieves a 20Gb/s data rate with 14ps peak-to-peak jitter and consumes 60mW from a 1.5V supply.

4.8 An 8Gb/s Transformer-Boosted Transmitter with $>V_{DD}$ Swing **5:00 PM**

J. Kim, University of California, Los Angeles, CA

An 8Gb/s serial-link transmitter that achieves $>V_{DD}$ signal swing without stressing the voltage tolerance of the transistors is presented. The high-frequency signal is boosted to large swings above the supply rail through multiple transformer coupling. The design is implemented in 1.2V 0.13µm CMOS technology. The prototype TX achieves $1.42V_{pp}$ output swing with 1.16V on-chip V_{DD} and draws 136mA. The S_{11} is less than -10dB for frequencies <4GHz.